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EXAMINER
RAY, G

E3M1/0702

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ART UNIT	PAPER NUMBER
2308	14

DATE MAILED: 07/02/93

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1-39 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☒ Claims 40 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-39 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed on _____, has been ☐ approved. ☐ disapproved (see explanation).
12. ☐ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

1. The examiner acknowledges the cancellation of claim 40 by the amendment filed on Feb. 16, 1993.

2. Claims 1-39 are presented for examination.

3. Claims 1-39 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner notes the following ambiguities.

As per claim 1, the phrase "a second plurality of uni-directional point-to-point buses for coupling in a second predetermined direction the output of the central unit to each of the bus elements" (lines 14-17) is vague and indefinite because it is unclear as to how one output of the central unit is connected to the second plurality of uni-directional point-to-point buses. clarification and/or rephrasing is required.

As per claims 2-29, the claims incorporate the deficiencies of the parent claim.

As per claim 30, the phrase "a plurality of second uni-directional point-to-point buses for coupling in a third predetermined direction the output of the combining logic to the central processing units" (lines 24-27) is vague and indefinite because it is unclear as to how one output of the combination logic is connected the a second plurality of uni-directional point-to-point buses.

As per claims 31-32, the claims incorporate the deficiencies of the parent claim.

As per claim 33, this claim recites a method. However, the claim has the same problems as in claim 1.

As per claims 34-39, the claims incorporate the deficiencies of the parent claim.

4. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

5. Claims 1-19 and 30-35 and 37-39 are rejected under 35 U.S.C. § 103 as being unpatentable over US Patent 4,837,682 issued to Culler in view of US Patent 5,168,547 issued to Miller et al.

As per claim 1, Culler teaches the claimed:

"a plurality of bus elements ...": Culler's plurality of bus elements ... (See Fig. 6, elements 508, 544, 548, 522 and 528);

"a central unit having a plurality of bus inputs and an

output": Culler's central unit having a plurality of bus inputs and at least one output (See Fig 5, element 600); and

"arbitration logic granting the bus elements through the central unit": Culler's arbitration logic granting access to bus elements (See col. 8, lines 36-42).

The difference between the instant claim and the reference of Culler is that the reference does not explicitly show the limitations of a "shared memory" and "a first plurality of uni-directional point-to-point buses ... and a second plurality of uni-directional point to point buses ..." (lines 11-17). However, Miller et al. in an analogous system teaches uni-directional buses (See Fig. 9, and col. 24, lines 65-66) and "shared memory" (Fig. 2b, elements 12c, 12d). It would have been obvious to one of ordinary skill in the data processing art at the time the invention was made to implement uni-directional buses and shared resources because such modification will help Culler's system to accomplish efficient high speed processing and to share valid updated information among users which are desirable features in any system. Applicant's submitted prior art WO-A-8 704 826 also shows uni-directional buses (See Fig. 2).

Furthermore, the above prior art does not explicitly show "coupling at least one of the inputs to the output". However, this can be interpreted as a "special interrupt" trying to get access directly by-passing an arbitration logic which is well

within the skill of ordinary person in the data processing art. Evidence of this is provided by US Patent 5,072,363 issued to Gallagher (See col. 2, lines 10-13). It would have been obvious to one of ordinary skill in the data processing art to implement the above feature in the above prior art of Culler in view of Miller because the prior art of Gallagher shows several types of arbitration scheme suitable for individual systems (See col. 2, line 61-col. 3, line 14 of Gallagher) and to select anyone is a matter of specific design choice.

As per claims 2-4, the limitations of the claims, i.e., "system further includes a state device" (claim 2), use of "OR gate" (claim 3), "multiplexer" (claim 4) do not patentably distinguish over the prior art because these are art recognized equivalents and thus it is a matter of specific engineering choice. The above concept is so well known that no reference is considered necessary. See MPEP 706.02a.

As per claims 5-19, these claims are rejected for similar reasons as in claims 2-4.

As per claim 30, this claim is rejected for similar rationale as in claim 1.

As per claims 31-32, these claims are rejected for similar reasons as in claims 2-4.

As per clam 33, this claim recites a method which parallels apparatus claim 1. In teaching the construction and use of the

device the prior art of culler in view of Miller inherently teaches a corresponding method.

As per claim 34, culler teaches the claimed:

"wherein the bus elements include a plurality of central processing units and a shared memory": Culler's bus elements include a plurality of central processing units and a shared memory (See Fig. 6).

As per claim 35, Culler teaches the claimed:

"selecting step further comprises selecting between the inputs on the first buses from the central processing unit and the bus from the memory": Culler's selecting inputs from the processors and memory (See col. 8, lines 12-25).

As per claims 37-38, these claims are rejected for similar reasons as in claims 2-4.

As per claim 39, Culler teaches the claimed:

"wherein a bus element includes a CPU": Culler's bus element includes a CPU (see Fig. 6, element 544).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gopal C. Ray whose telephone number is (703) 305-9647.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Gopal C. Ray

GOPAL C. RAY
PATENT EXAMINER
GROUP 2300